

LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A flip chip semiconductor device comprising a silicon wafer having parallel first and second major surfaces; at least one P region and at least one N region in said wafer which meet at a PN junction within said silicon wafer; first and second laterally spaced and metallized layers formed on said first major surface and each connected to one of said P region and said N region; a bottom metallized layer extending across said second major surface; and

a third metallized layer atop said first major surface which is laterally spaced from said first and second metallized layers; said first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgated device, wherein a current path inside said silicon wafer from said source electrode to said drain electrode includes a vertical component which is generally perpendicular to said first major surface.

2. (Canceled)

3. (Original) The device of claim 1 which further includes at least one contact bump connected to each of said metallized layers.

4. (Previously Presented) The device of claim 1 which further includes at least one contact bump connected to each of said metallized layers.

5. - 7. (Canceled)

8. (Original) The device of claim 4 wherein said bottom metallized layer is substantially thicker than all of said first and second metallized layers.

9. (Previously Presented) The device of claim 1 wherein a plurality of contact bumps are connected to each of said first and second metallized layers; said plurality of contact bumps connected to said first metallized layer being aligned along a first straight row; said plurality of contact bumps connected to said second metallized layer being aligned along a second straight row.

10. (Original) The device of claim 9 wherein said first and second rows are parallel to one another.

11. (Canceled)

12. (Previously Presented) A flip chip semiconductor device comprising a silicon wafer having first and second parallel major surfaces; at least one P region and at least one N region in said wafer which meet at a PN junction within said silicon wafer; first and second laterally spaced metallized layers formed on said first major surface and each connected to one of said P region and said N region; a third metallized layer atop said first major surface which is laterally spaced from said first and second metallized layers; said first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgated device; and a plurality of contact bumps connected to each of said first and second metallized layers; said plurality of contact bumps connected to said first metallized layer being aligned along a first straight row; said plurality of contact bumps connected to said second metallized layer being aligned along a second straight row, wherein a current path inside said silicon wafer from said source electrode to said drain electrode includes a vertical component which is generally perpendicular to said first major surface.

13. (Canceled)

14. (Previously Presented) The device of claim 12, further comprising a bottom metallized layer extending across said second major surface.

15. (Previously Presented) The device of claim 14, wherein said bottom metallized layer is substantially thicker than all of said first and second metallized layers.

16. (Previously Presented) The device of claim 12, wherein said first and second rows are parallel to one another.

17. (Previously Presented) The device of claim 12, wherein said silicon wafer is a rectangular wafer having an area defined by a given length and a given width, said length being greater than said width; said first and second rows of bumps being parallel to one another and being symmetric about a diagonal line across said wafer.

18. (Canceled)

19. (Previously Presented) The device of claim 14, wherein said silicon wafer is a rectangular wafer having an area defined by a given length and a given width, said length being greater than said width; said first and second rows of bumps being parallel to one another and being symmetric about a diagonal line across said wafer.

20.-26. (Canceled)

27. (Previously Presented) A semiconductor device comprising a silicon die having first and second parallel surfaces; a region of one conductivity type extending from said first surface and into the body of said die; a junction pattern defined in said device formed by a plurality of laterally spaced diffusions of the other conductivity type into said region of one conductivity type; a first conductive power electrode formed atop said first surface and in contact with said plurality of laterally spaced diffusions; a second conductive power electrode formed atop said first surface which is laterally spaced from said first conductive electrode and in electrical contact with the body of said die through a high conductivity element; and at least one solder ball connector formed atop each of said first and second conductive electrodes

respectively; the current path inside said silicon die from said first conductive electrode to said second conductive electrode having a vertical component which is generally perpendicular to said first surface.

28. (Original) A semiconductor device according to claim 27, wherein said high conductivity element is a sinker diffusion of higher conductivity than said body region.

29. (Original) A semiconductor device according to claim 27, wherein said high conductivity element is a metallic material residing in a trench formed in said body of said die.